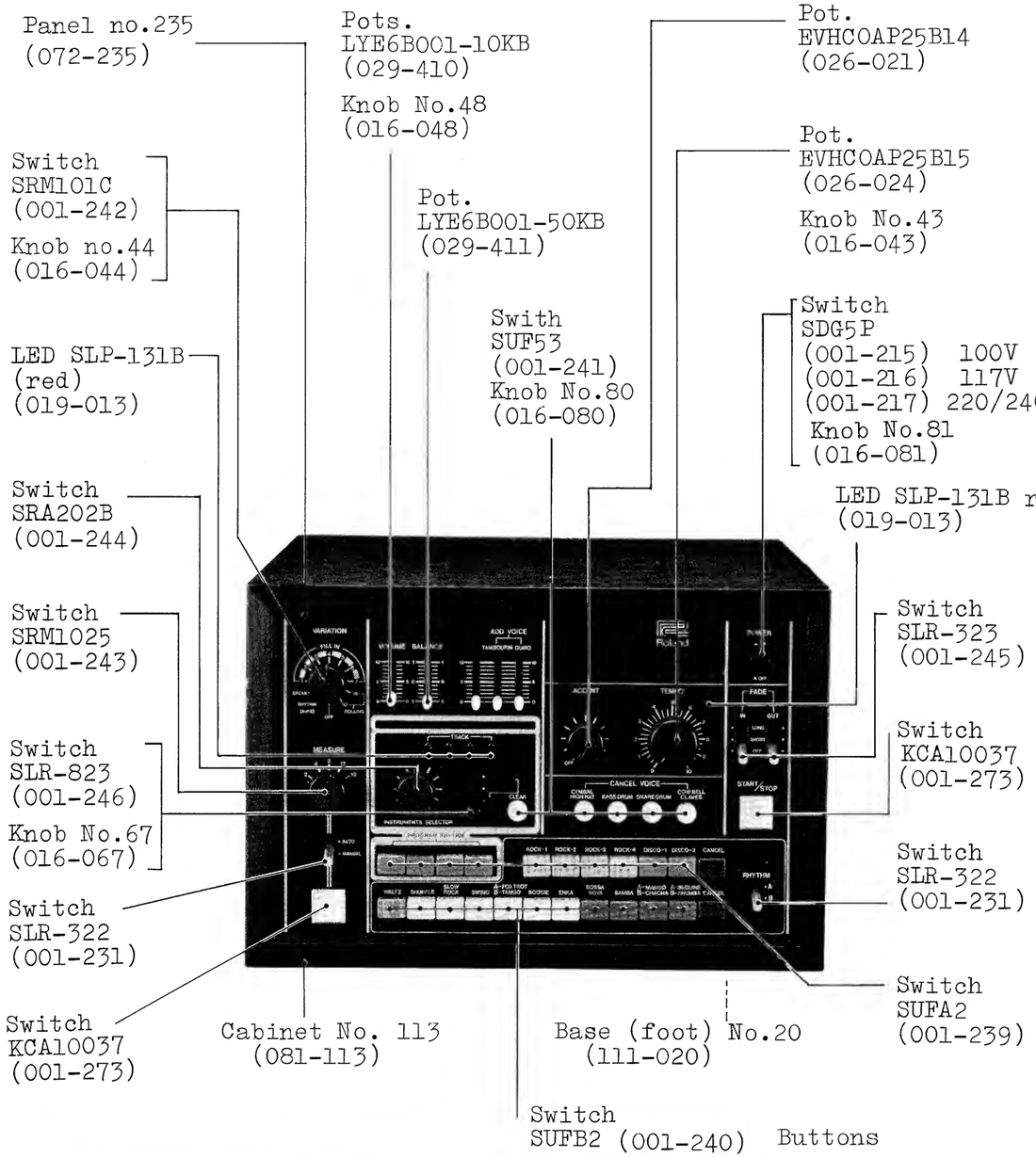
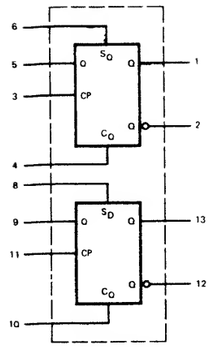
CR-78 SERVICE NOTES

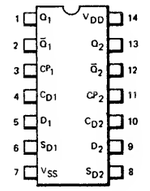


LOGIC SYMBOL
F4013



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4013 TRUTH TABLES

SYNCHRONOUS INPUTS		OUTPUTS	
CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
⌐	L	L	H
⌐	H	H	L

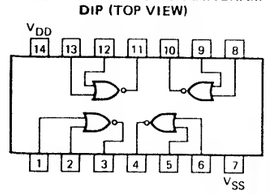
Conditions: S_D = C_D = LOW

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	L	L

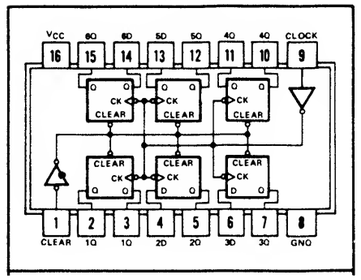
L = LOW Level
H = HIGH Level
⌐ = Positive-Going Transition
X = Don't Care
Q_{n+1} = State After Clock Positive Transition

F4001 QUAD 2-INPUT NOR GATE

F4001
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

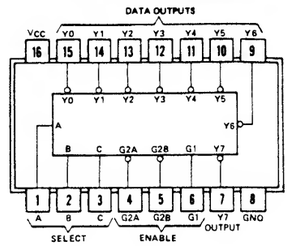


SN74LS174, SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE SN74174, SN74LS174, SN74S174 . . . J OR N PACKAGE (TOP VIEW)

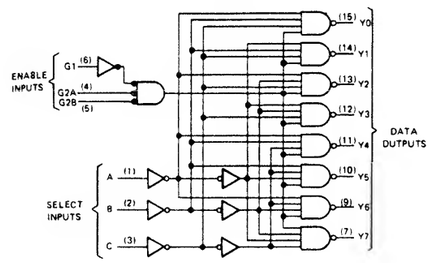


DECODERS/DEMULTIPLEXERS

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)



'LS138, 'S138



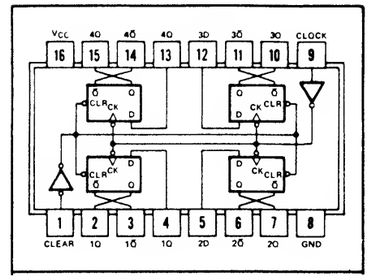
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

SN74LS175, F40175

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE
(TOP VIEW)



NOTE:
In using F40175, refer to note on page 8.

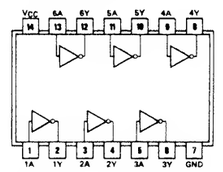
QUADRUPLE D-TYPE FLIP-FLOPS

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

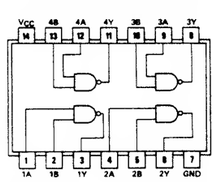
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

HEX INVERTERS



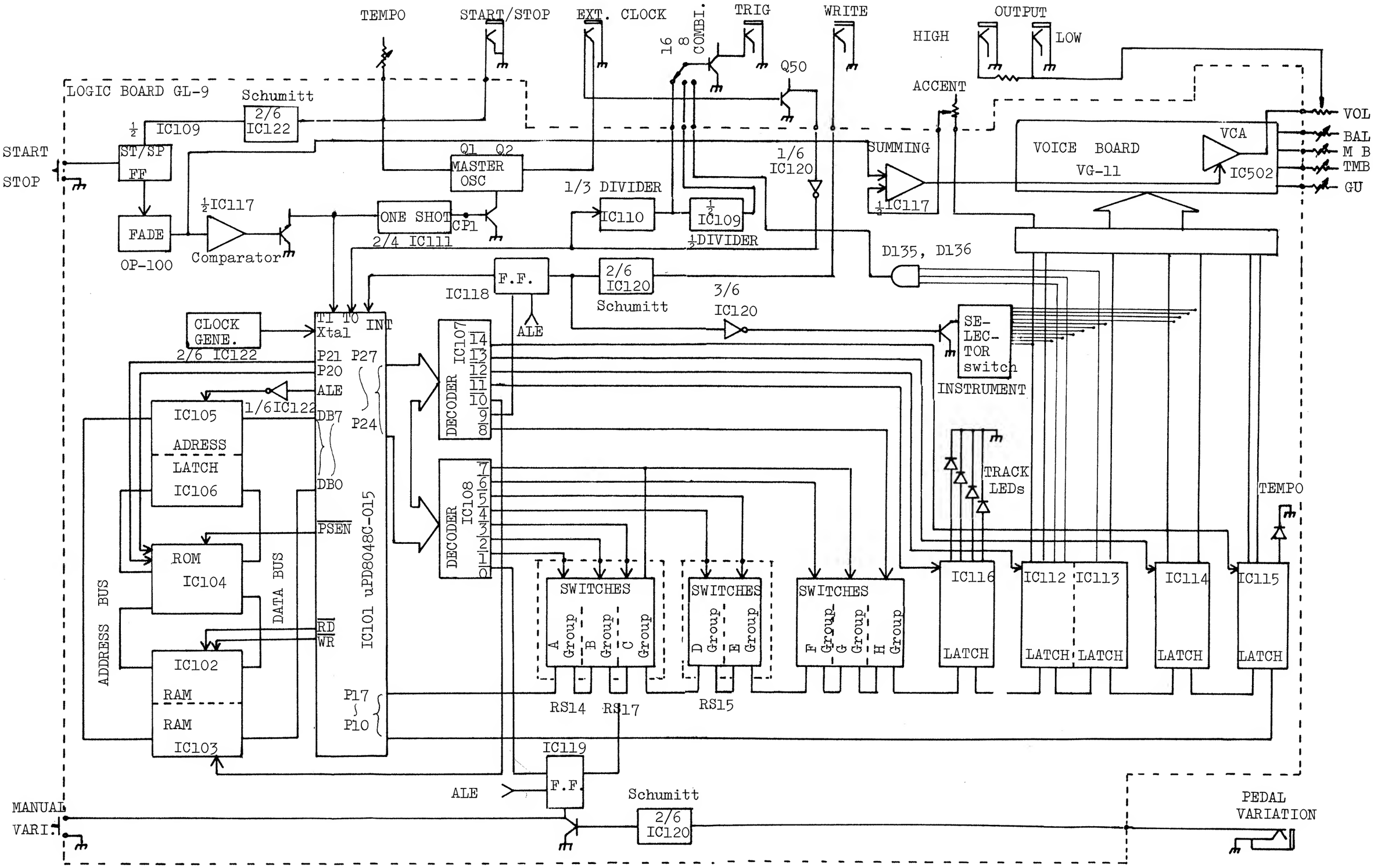
SN5404 (J) **SN7404 (J, N)**
SN54H04 (J) **SN74H04 (J, N)**
SN54L04 (J) **SN74L04 (J, N)**
SN54LS04 (J, W) **SN74LS04 (J, N)**
SN54S04 (J, W) **SN74S04 (J, N)**

QUADRUPLE 2-INPUT POSITIVE-NAND GATES



SN5400 (J) **SN7400 (J, N)**
SN54H00 (J) **SN74H00 (J, N)**
SN54L00 (J) **SN74L00 (J, N)**
SN54LS00 (J, W) **SN74LS00 (J, N)**
SN54S00 (J, W) **SN74S00 (J, N)**

CR-78 BLOCK DIAGRAM



SPECIFICATIONS

OUTPUT IMPEDANCE

H: 220k ohms L: 10k ohms

OUTPUT LEVEL

H: 3.5Vpp into 220k

L: 5.5Vpp into 10k
(VOL. ACC. max)

TRIGGER: +15V

EXT. CLOCK

+5V--- +15V
min. 5ms in length

POWER CONSUMPTION

9W (117V)

13W (220/240V)

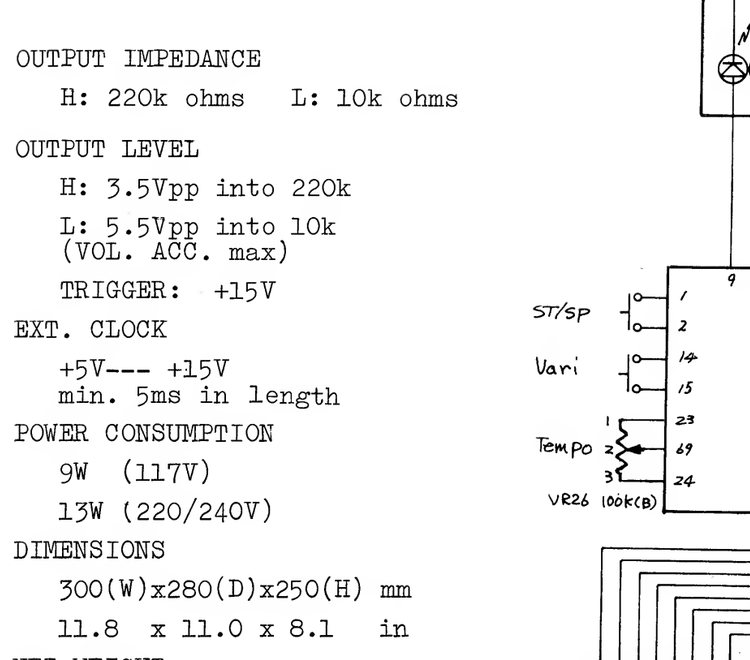
DIMENSIONS

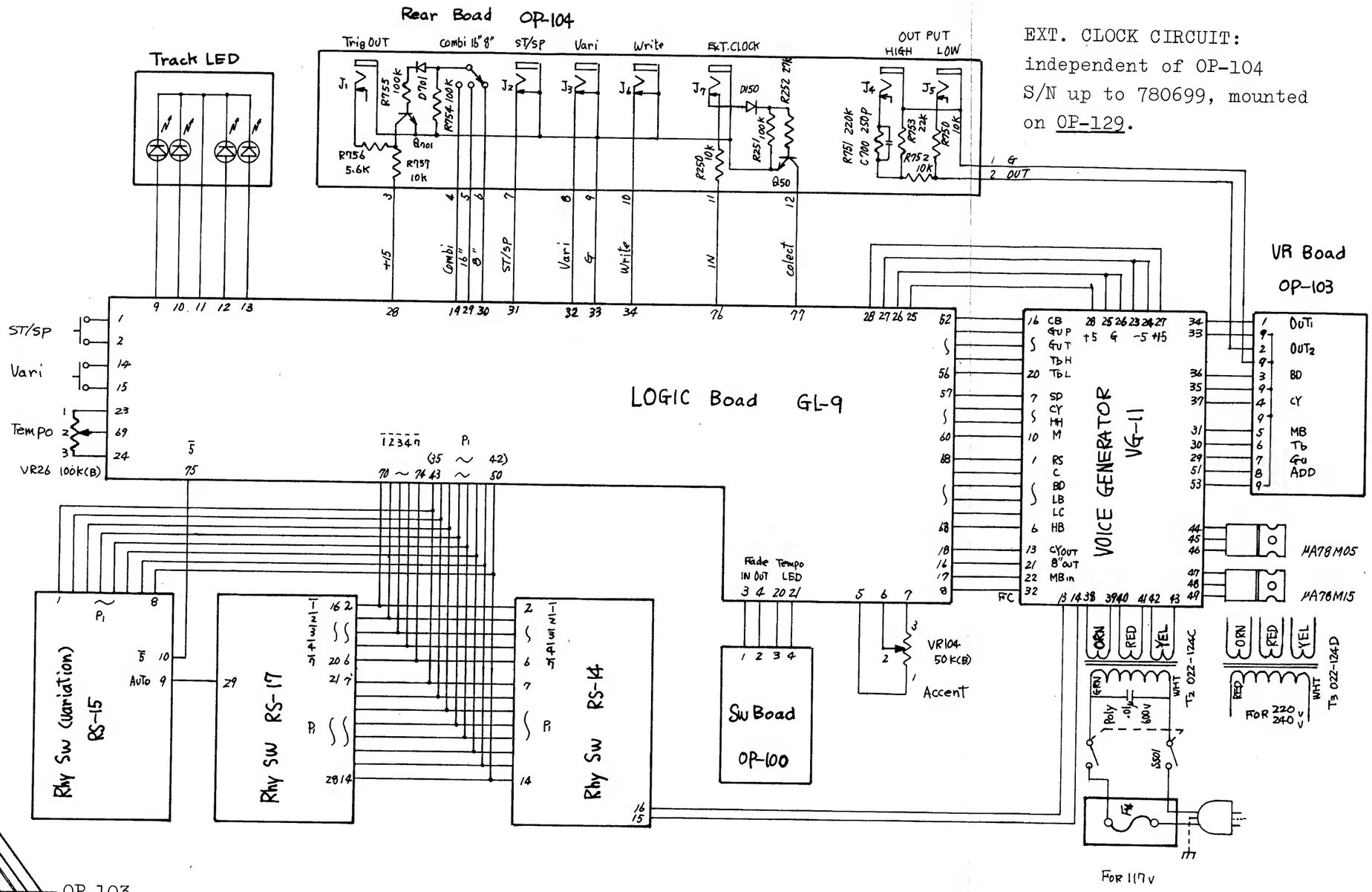
300(W)x280(D)x250(H) mm

11.8 x 11.0 x 8.1 in

NET WEIGHT

5.5Kg 12.1 lbs

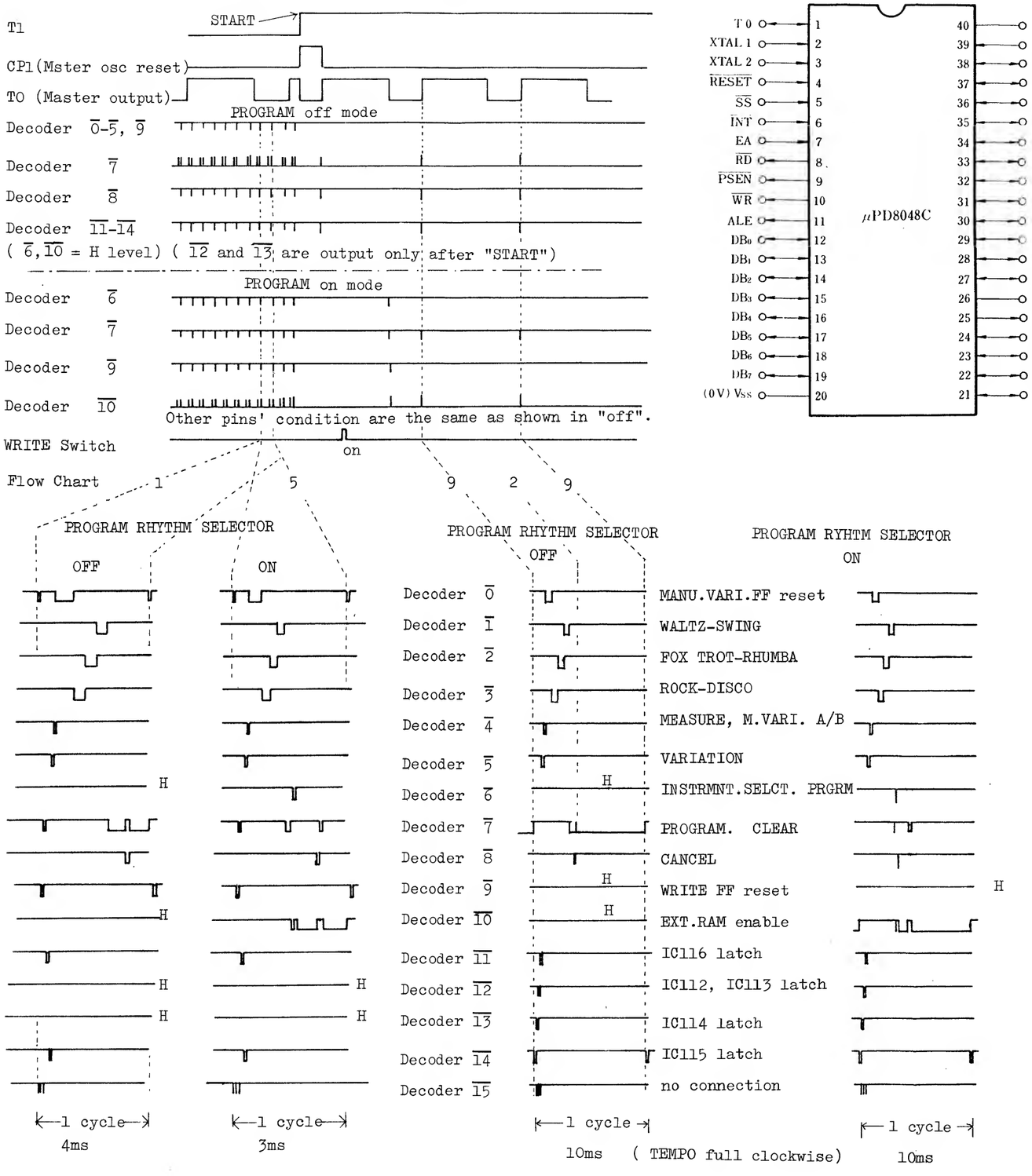




FUSES RATING

F1 (-5V)	F2 (+15V)	F3 (+5V)	F4 (prim.)
SGA 0.125A (008-022)	SGA 1A (008-026)	SGA 0.5A (008-024)	SGA 0.5A (008-024)
CEE T50mA (008-053)	CEE T250mA (008-060)	CEE T400mA (008-062)	CEE T250mA (008-060)

CR-78 CIRCUITS TIMING DIAGRAM



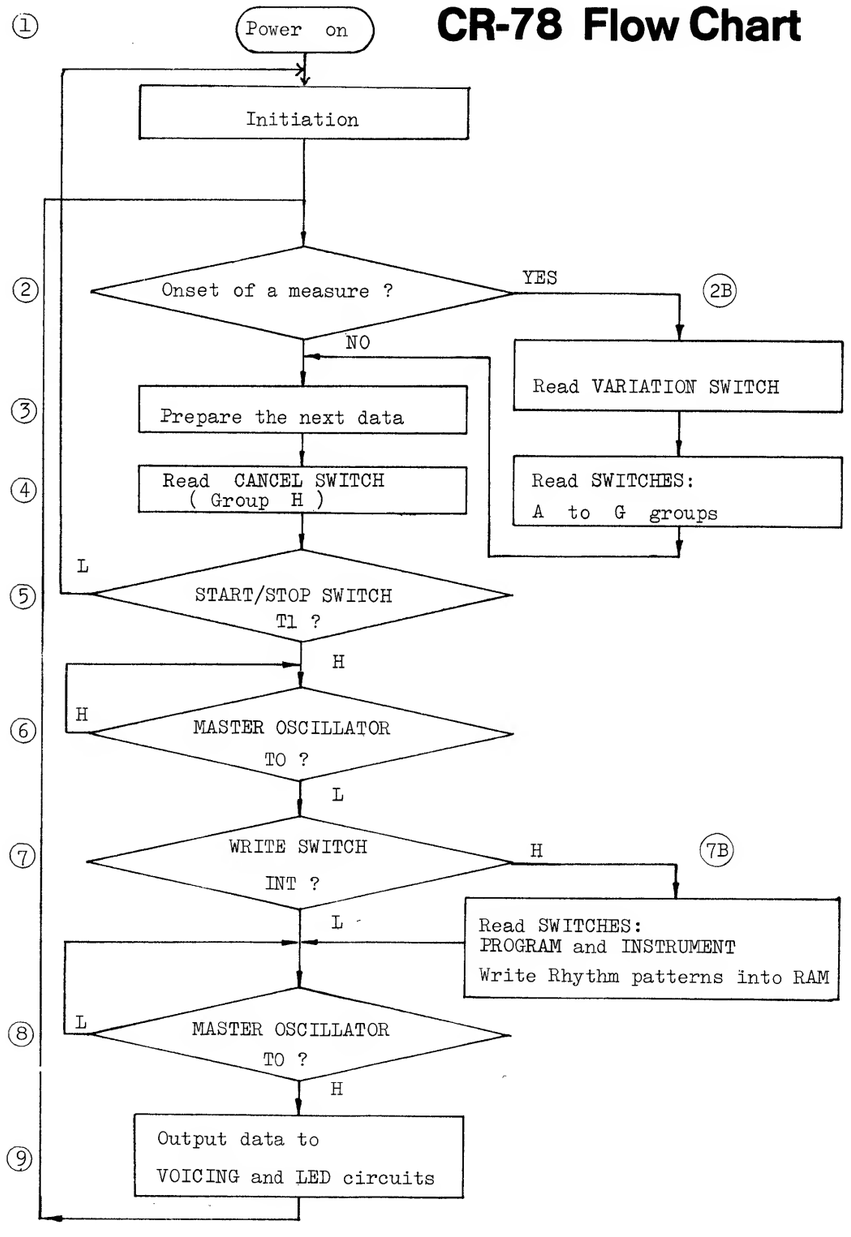
μPD8048

(Top View)

One chip michrocomputer μPD8048C—015

The μPD8048 is an 8-bit parallel computer fabricated on a single sillicon chip. The 8048 contains a 1k x 8 ROM program memory, a 64 x 8 RAM memory, 27 I/O lines, an 8-bit timer/counter and clock circuits.
Used in the CR-78 is a μPD8048C-015 version in which the programs and data dedicated to the CR-78 are stored in program memory.

CR-78 Flow Chart



CIRCUIT DESCRIPTION

The CR-78 is a computerized rhythm machine whose rhythms are controlled by the resident computer through internally stored programs. Rhythms other than stored can be programed as desired by using the built-in expansion ROM and RAMs. Sequential program order is outlined in the flow chart and the timing diagram shows relationship among principal circuits waveforms. (see previous page) The following description is composed of two sections: General Introduction and Detailed Function. Title numbers refer to those in flow chart.

GENERAL INTRODUCTION

1. POWER ON

When power is first applied, two oscillators start oscillation: MASTER OSCILLATOR, determines rhythm tempo, ranging from 5Hz to 100Hz; CLOCK GENERATOR, generates timing pulses for the 8048 in each step cycle.

2. 2B. SWITCH SANNING

Even in the stop mede, the computer needs to store a data on switching status so as to output rhythm patterns immediately after the START/STOP switch is depressed. And also a status data is needed at the beginning of a measure.
The switch reading to obtain a switch set-up data is refereed to as switch scanning.
From Port 2 of 8048, signals are routed through the Decoders IC107 and IC108, and the switch matrix to Port 1. Combination of two port's pins according to switch settings becomes a data on switch status. After a rhythm runs, scanning is done onee for each measure.

3. PROCESSING and PREPARING DATA

The 8048 prepares the next data according to the internal program based on switch scanning data.

4. SCANNING CANCEL VOISE SWITCH

Since switch scanning is performed once for one measure during rhythm running, switching during the measure is effective in the subsequent measure. However, "CANCEL VOICE" is scanned every cycle to cancel the unwanted voice at once whenever it is specified.

5. SENSING START/STOP SWITCHING

As long as T1, the START/STOP sensing input terminal of μPD8048 is kept low, the program routine is not allowed to break loop through 1-5, returning to 1. When the START/STOP switch is pushed while a rythm stops, T1 is pulled to high to start a rhythm and falls to low when the START/STOP is pushed again(stop)

6. SENSING MASTER OUTPUT FALLING

Although each circuit operates its given task in sequence under the control of timing pulses from the CLOCK GENERATOR, each program step must keep pace with oscillation of the master osc. (rhythm tempo) by sensing the falls and rises of waveforms of the master oscillator.
A program step proceeds to the next step when the master's trailing edge goes to negative.

7. SENSING WRITE SWITCHING

When the WRITE switch is tapped, the write hold circuit IC118 is set, applying high level to INT, and causing program routine to jump to 7B.

7B. WRITING PROGRAM RHYTHM

Scanning signals from $\overline{6}$ and $\overline{7}$ of the decoder IC-108 tell the computer which position of INSTRUMENT and which PROGRAM push switch is selected. Then the data on PROGRAM rhythm are stored into the RAMs IC102 and IC103 under the control of a program from the ROM IC104. The RAMs provide memory size for two measures for each voice.

8. SENSING MASTER RISING

The computer executes a program, synchronizing its step with a rhythm tempo. As soon as T0 receives the rise of a master square, 8048 starts to produce rhythm patterns by sending data and control signals out from Port 1 and 2.

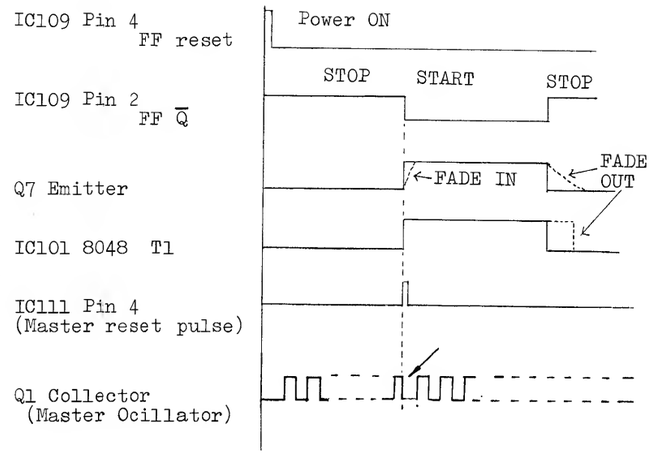
9. OUTPUTTING DATA

The Port 1 this time serves as an output port, feeding data for rhythm patterns (VOICES) and LEDs (TRACK) to the latches IC112-IC116 which selectively latch them in sequence under the control of signals coming from the Port 2 through the Decoder IC107. The computer performs the entire loop once for one cycle of master oscillator and 48 times per measure.

FUNCTION —Detail—

1. POWER ON

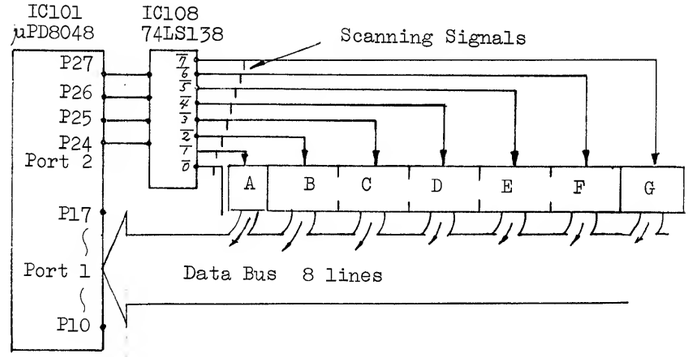
Resetting of the START/STOP flip-flop IC109A inhibits a rhythm from running by holding T1 of μPD8048 at low level until the START/STOP switch is first tapped.
When power is on, since the both pins 12 and 13 of IC111A are grounded momentarily, its output (pin 11) level swings to high resetting the RS flip flop IC109A which in turn develops high output at pin 2, setting T1 level to low (through Q5-Q7, IC117A and Q11). Pins 12 and 13 of IC111 will go positive as C103 charges, but IC-109A output is kept high until the START/STOP switch is depressed.



2. NO DETAIL

2B. SWITCH SCANNING

Switch scanning cycle initiates to generate internally programed binary signals from the Port 2, P24-P27, feeding them to IC108, binary-to-hexadecimal decoder, from which decoded signals are routed to respective switch groups. From the decoder only one pin outputs negative going pulse while the rest pins output H, and the next pin outputs H with the rest L. These outputs of signals occur in sequence within a time interval of microseconds and repeats over and over again every few milliseconds until the START/STOP switch is depressed to run the rhythm. After running, scanning siganls are outputed once at the onset of a measure.
This means that changing of any switch setting during a measure is ignored by the computer unless switch setting is kept unchanged until the next scanning.
Similarly, changing the MEASURE of VARIATION in AUTO mode will be made into effective only after previousely specified measure(s) has passed.

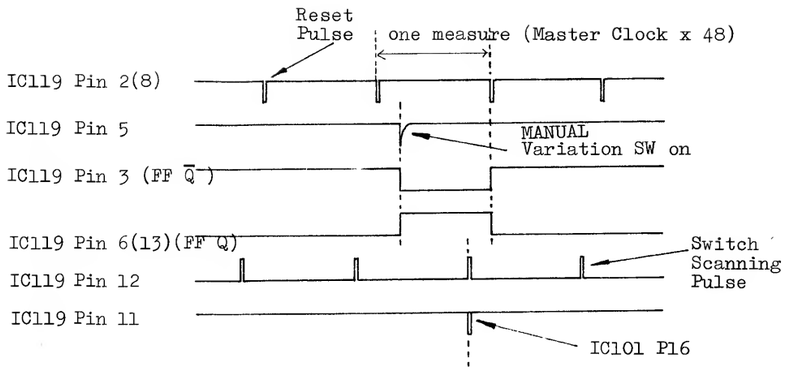


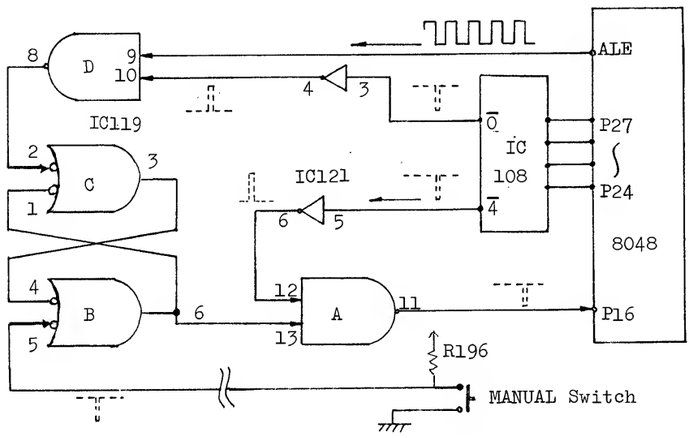
In MANUAL mode, VARIATION change during a measure is enabled at the beginning of the next measure by holding that changing information until the next scanning is performed.

For this purpose the MANUAL VARI hold circuit is used which consists of IC119. When the START/STOP switch is pressed while a rhythm stops, the RS flip flop IC119 (pins 1-6) is reset by a pulse from $\overline{0}$ of IC108, switching pin 3 to H and pin 6 to L.

Depressing the MANUAL switch during rhythm running sets the FF IC119A/B, holding pin 6 or pin 13 at H. When a master output goes low, a scanning pulse is generated from $\overline{4}$ of IC108, after inverted by IC121, it is NANDed with pin 13 input, causing pin 11 to develop a negative going pulse which is detected by the 8048 through P16, this is MANUAL "ON" information.

After scanning, a reset pulse is applied from $\overline{0}$ of IC108 to pin 2 through the NAND circuit IC119D.





3. NO DETAIL

4. NO DETAIL

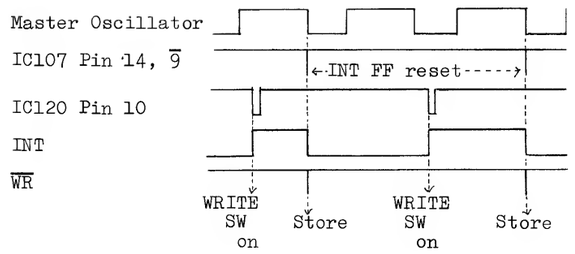
5. SENSING START/STOP SWITCHING

The START/STOP FF IC109A receives a positive going pulse each time the START/STOP switch is pushed, switching its output H or L and holding it until the next push is made.
Pushing the START/STOP switch applies a positive pulse to pin 3 of the START/STOP FF IC-109A causing it to have a high or low output until the START/STOP switch is pressed again.
The output from the FF is applied through Q5, Q6 and OP-100 to pin 6 of the comparator IC117A which provides a reference voltage at pin 5.
When an input to pin 6 of the comparator exceeds the reference voltage of pin 5, the comparator senses it, sending output to:
1. T1 of 8048 to start the rhythm,
2. the master oscillator and 8 and 16 beat dividers IC109B and IC110 through the one shot pulse generator IC111 (pins 1-6) to reset them and to synchronize their starts.
When the voltage at pin 6 of the comparator drops below the reference voltage, low output is applied to T1 to stop the rhythm.

However, if the FADE IN or FADE OUT switch is in closed position, voltage swing at T1 is delayed behind START/STOP switching due to the time constant in the fade circuit.(detailed later)

6. MASTER OSCILLATOR

The master oscillator output waveform has a duty ratio of over 50%.
When the WRITE switch is tapped, the WRITE FF IC-118 is set, applying high output to INT pin of 8048 which will go low when the master output falls. This is a "WRITE ON" information to the computer, upon receiving the "write on" information, switch scanning pulses are sent from $\overline{0}$, $\overline{7}$, $\overline{9}$ and $\overline{10}$ of the decoders and associated data are memorized into external RAMs IC102 and IC103. The circuit configuration and function of the WRITE FF are much the same as in the MANUAL FF except for reset timing.
As shown in the figure, whenever the write switch is tapped, as long as it is occured during master's high level period, information is recognized by the computer when the master output falls, however, if the write switch is tapped during low level period, it is treated as it is occured during the next high level period, and then, sound is reproduced, being delayed by $\frac{1}{2}$ cycle of the master oscillator.
The longer high level period of the master oscillator waveform is intended to compensate for delayed timing of key operation.



7. NO DETAIL

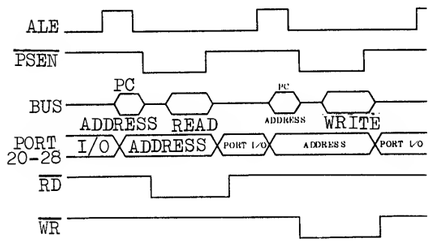
7B. WRITING PROGRAM RHYTHM

As described in section 6, when the write switch is tapped during a measure, information on PROGRAM rhythm are stored in RAMs at the sbsequent master square trailing edge, and INT of 8048 receives H input from the write hold circuit which consists of IC118 which functions in the same way as in the MANUAL VARI.(in this case reset pulse is fed from pin 14 or $\overline{9}$ of IC107).
When the write switch is depressed during a measure, H level is applied at INT pin and is held until master falls, this is "write on" information, and the computer detects through switch scanning (pulses from $\overline{6}$ and $\overline{7}$ of IC108) which of PROGRAM switches and which position of INSTRUMENT switch is selected.
The selected INSTRUMENT is first stored into RAM, then rhythm patterns are stored.
When the same instrument has been addressed in the RAM track, rhythm patterns being written are added to the patterns previously stored in the RAM and will not be stored in another track independently.
Required bit numbers for two measures are:
4 (PROGRAM) x 4 (INSTRUMENT) x 96 steps (48 x 2) = 1536 bits.
Data transfer to/from RAMs and ROM are performed as follows:
ALE (Address Latch Enable)
This signal occurs once for 15 Clock Generator frequency, that is, 250kHz, and latches address being outputed from DB, through internal program, delivering the latched signals to RAMs and ROM.

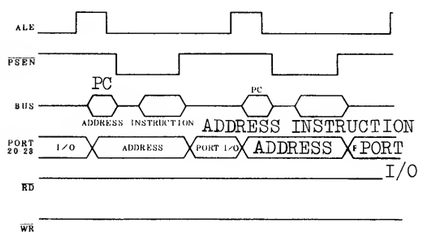
ROM (IC104)
Program memory addressed by the address signals from the lateches IC105, IC106 and P20 and P21 is fetched when $\overline{PSEN}$ is low at 2B and 7B of the flowchart.

RAM (IC102, IC103)
Stored data are read when $\overline{RD}$ is low at 2B and 7B of the flow chart. Information are stored when $\overline{WR}$ is low at 7B of the flow chart.

CYCLE TIMING FOR EXTERNAL DATA MEMORY (RAM) WRITE/READ



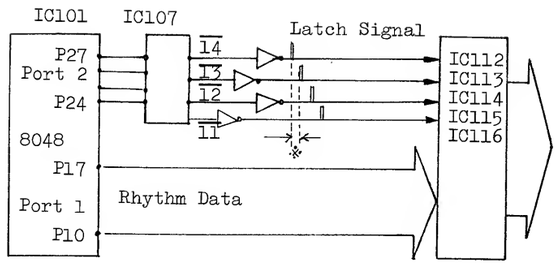
CYCLE TIMING FOR EXTERNAL PROGRAM MEMORY (ROM) READ

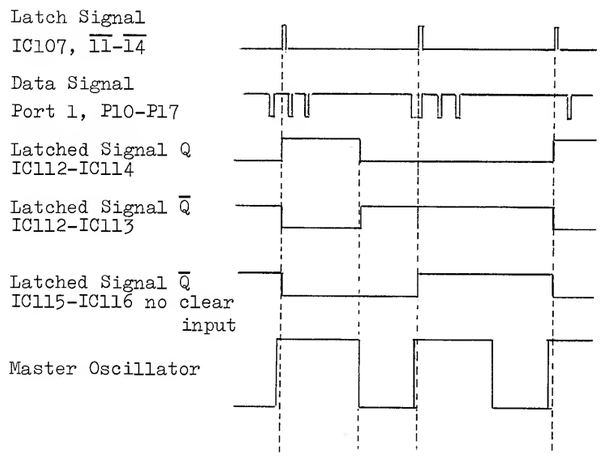


8. 9. DATA OUTPUT
- LATCH CIRCUITS -

When the program proceeds at data output routine, Port 1 this time acts as an output port since it is a bidirectional port, representing the data through internal program memory or external ROM and RAMs, data are sent from P10-P17 to IC112-IC116 latch circuits whose clock input pins receive latch signals from port 2 via decoder IC107. When a latch pulse goes positive while a data signal is fed onto the clock pin, the data is latched and sent to the VOICING circuit or LED. When the latched data is for voicing, it is applied after inverted and amplified by a buffer.
There are three kinds of latched outputs, as the master output goes negative, Qs and $\overline{Q}$s of IC112-IC114 are cleared, maintaining their pulse lengths almost the same as the master wave length.
On the other hand, $\overline{Q}$s of IC115 and IC116 are held L until the next latch signal comes since these clear pins of IC115 and IC116 are not connected to the master oscillator output.

Note: since the time interval between pulses within the arrows marked by * is 70μs, they are considered to occur at the same time.





= FADE and ACCENT =

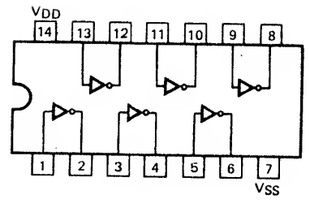
As described in section 4, the FADE circuits on OP-100 are enabled when the FADE IN and/or FADE OUT swithches are turned on to make the rhythm sounds gradually louder (VCA) as a rhythm starts and to stop the rhythm (T1) as sounds die away.
These timings are determined by the RC constants in the FADE circuits.
Accent pulses are also affected by the FADE circuits in amplitude ratio and are mixed with the sound control voltage in the summing amp. IC117 from which incorporate control voltages are sent to the VCA on the VG-11 to control rhythm volume.

= SOUND KILLER =

These circuits "kill" undesired sounds resulted from transient voltages on their way to output:
1. When power is on, Q512 on the VG-11 is not supplied enough collector voltage to amplify a input signal until C558 charges to some extent.
2. When power is off, C558 discharges through Q535 and Q532 on the VG-11, grounding pin 1 of VCA IC502.
3. The circuit comosed of Q12 and Q13 on the GL-9 is identical and functions in the same manner as the circuits described above, but is used to protect the RAMs and to prevent disorderly running of 8048.

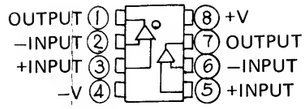
MC14069BCP

DIP (TOP VIEW)

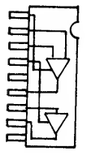


μPC4558

TOP VIEW



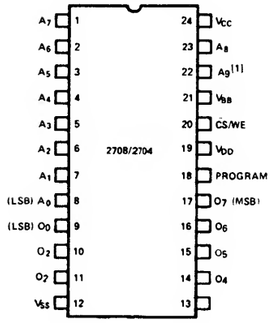
BA662



5 − V
9 + V

AM2708P

PIN CONFIGURATION

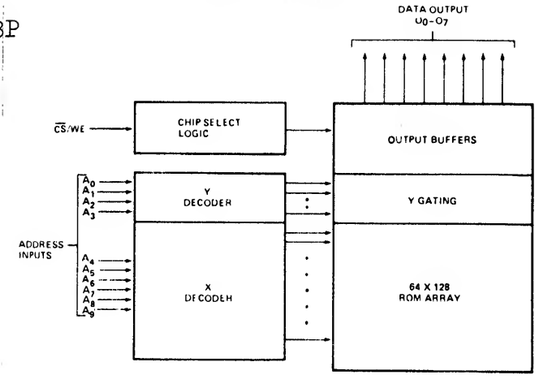


NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

PIN NAMES

A_0 A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

BLOCK DIAGRAM

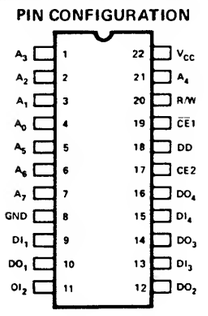


PIN CONNECTION DURING READ OR PROGRAM

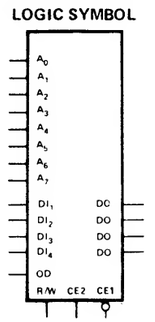
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1 B, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

μPD5101C-E

PIN CONFIGURATION



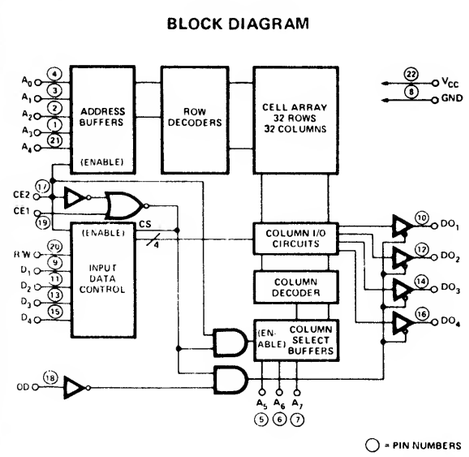
LOGIC SYMBOL



TRUTH TABLE

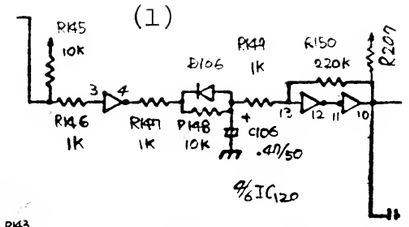
$\overline{CE_1}$	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

BLOCK DIAGRAM

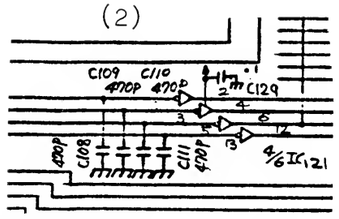


GL-9A (142-009A)
(Etch mask 052-438A)
Serial No. 780700-821050
Use GL-9B for replacement

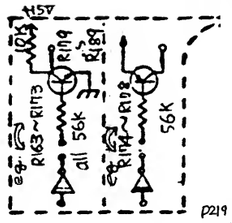
(1)

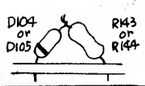


(2)

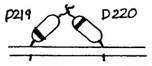


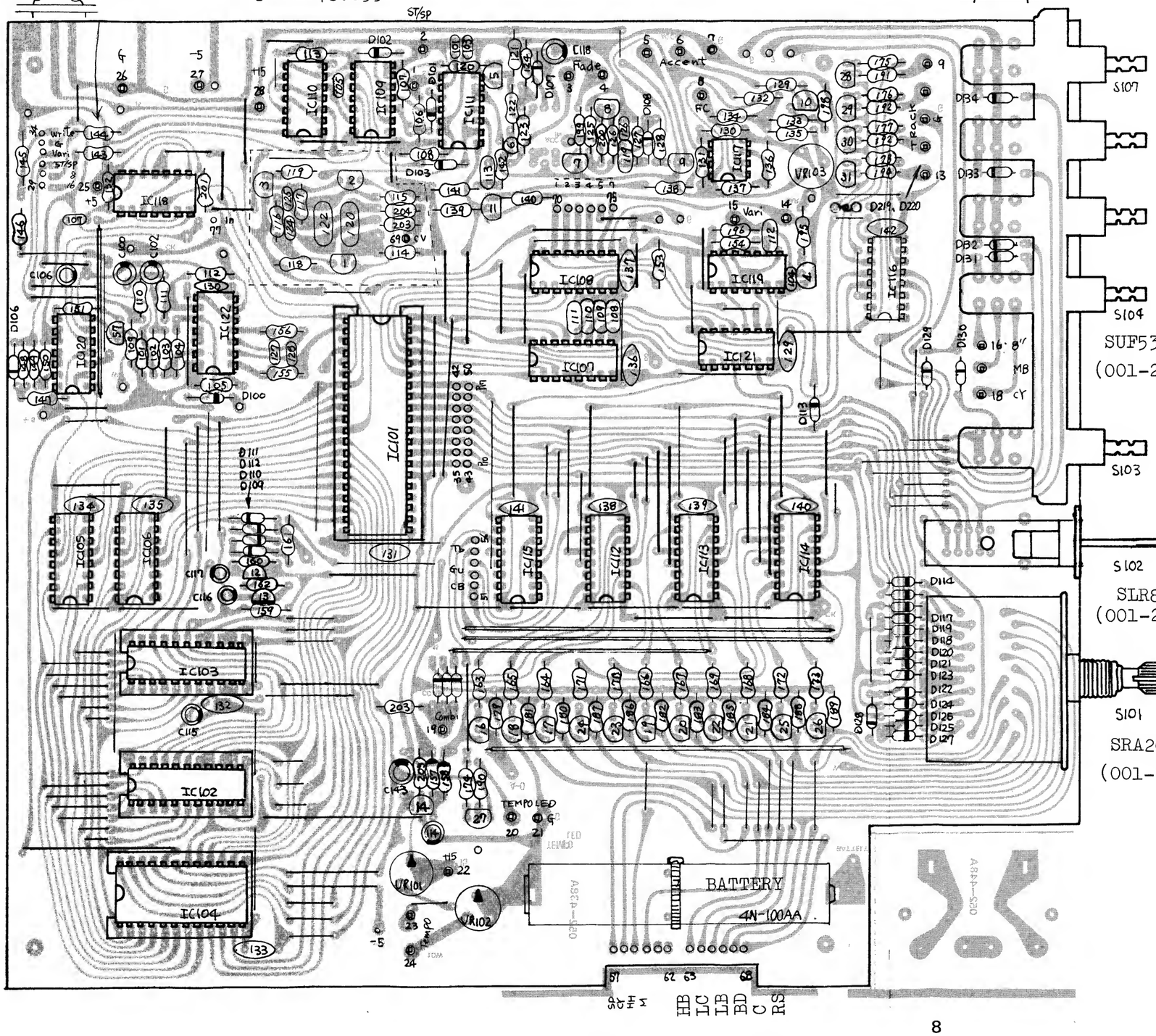
(3)





Serial no. up to 780699

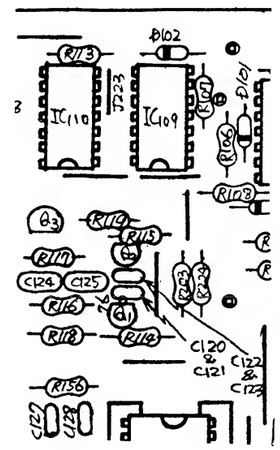




SUF53
(001-241)

SLR823
(001-246)

SRA202B
(001-244)



GL-9 only

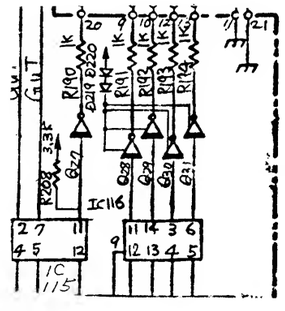
Serial no. up to 780699

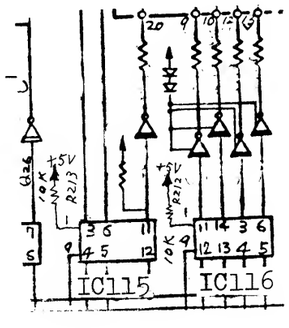
GL-9 Circuit Board is the same as GL-9A except for portion shown left and following parts are attached on the foil side.

R202, R201, R105, C105

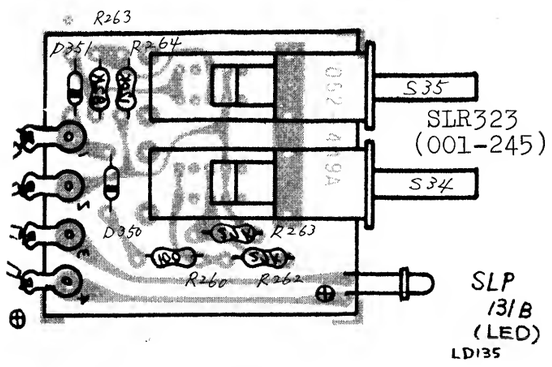
For the decoder (IC112, 113, 115,116) two kinds of logic IC are available;
TTL (74LS175, or equiv.) and CMOS (74C175, 14175, or equiv.).
When CMOS type is used as a replacement for TTL, pin 1 of IC115 and IC116 must be connected to +5V supply through a 10k-ohm as shown in below right (R212, R213).
When TTL is used, the 10k ohms resistors become optional.

(4)

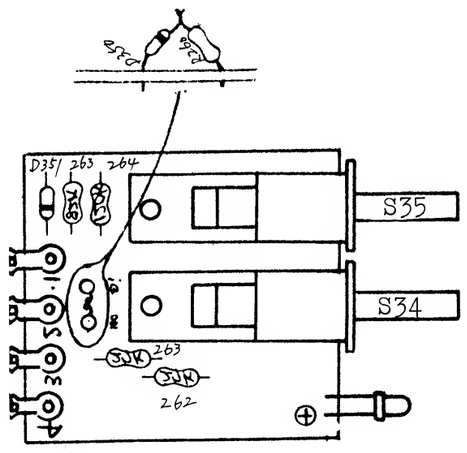




OP-100A (149-100A)
(Etch mask 052-449A)



view from foil side

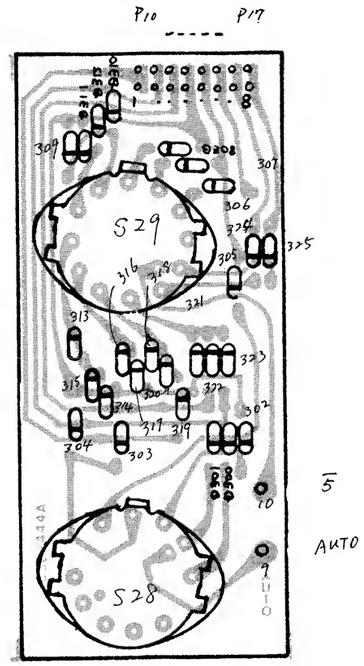


OP-100

Serial no. up to 780699

Use OP-100A for replacement

RS-15A (148-015A)
(Etch mask 052-052-444A)



view from foil side

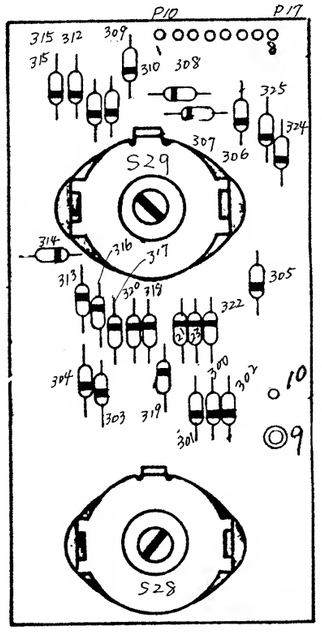
RS-15

Serial no. up to 780699

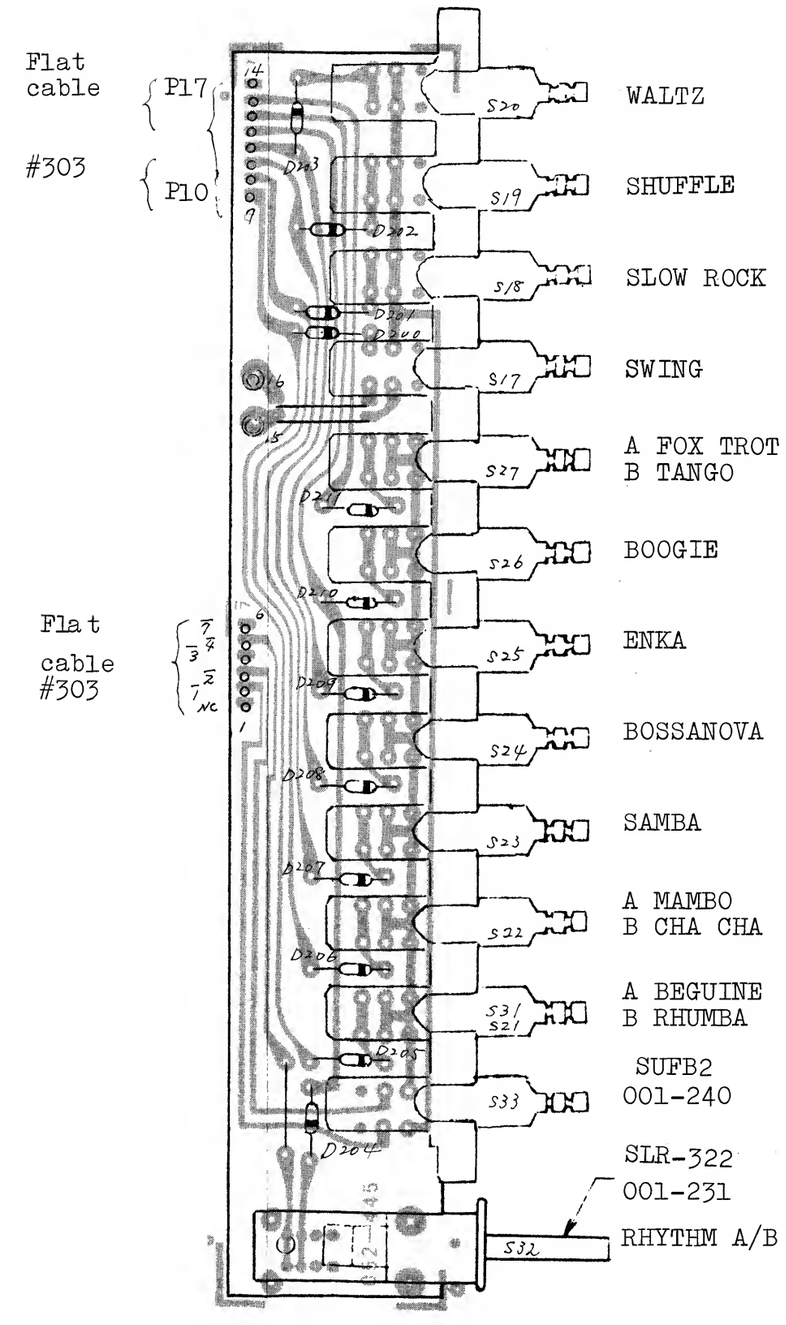
Use RS-15A for replacement

SRM101C
(001-242)

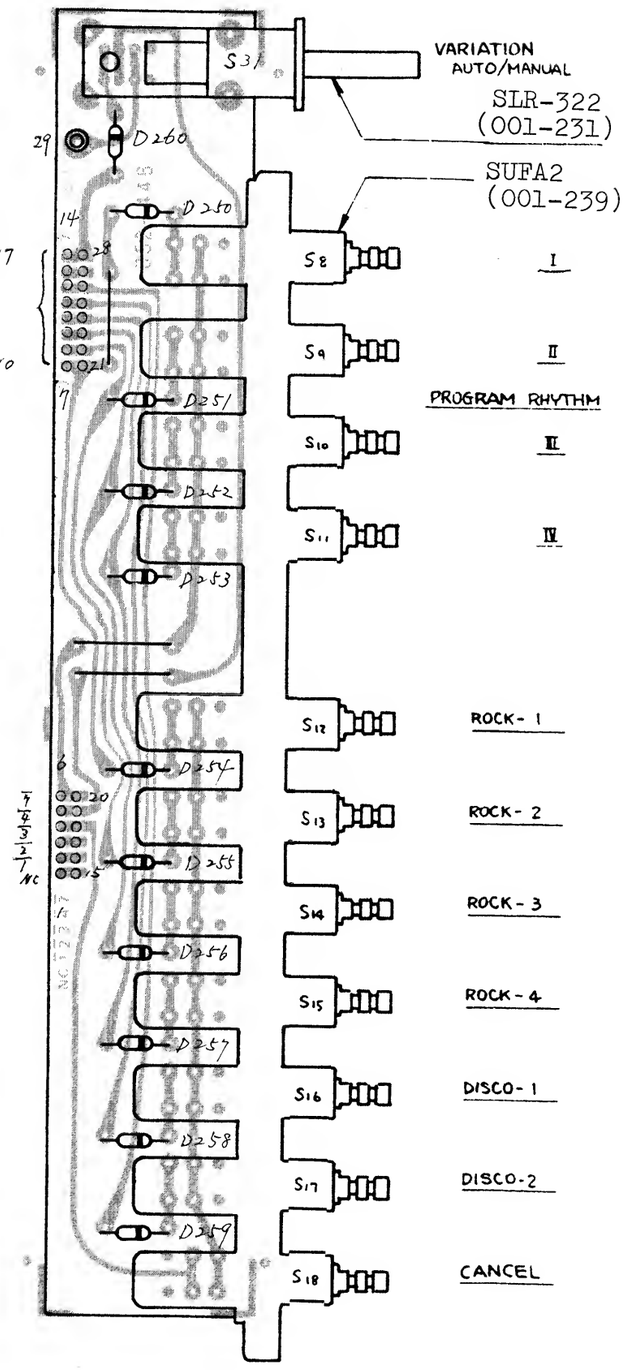
SRM1025
(001-243)



RS-14 (148-014)
(Etch mask 052-445)
view from foil side

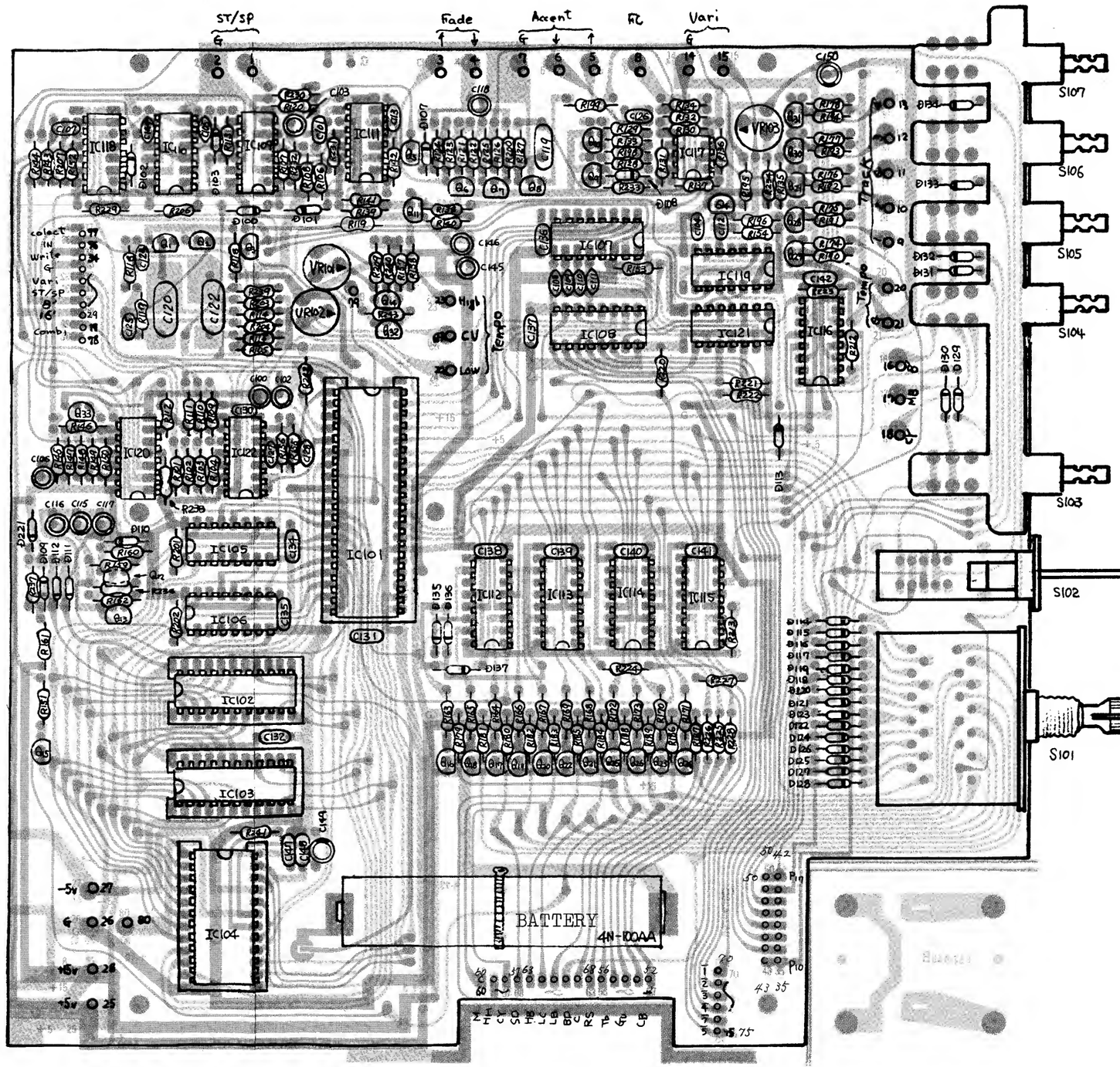


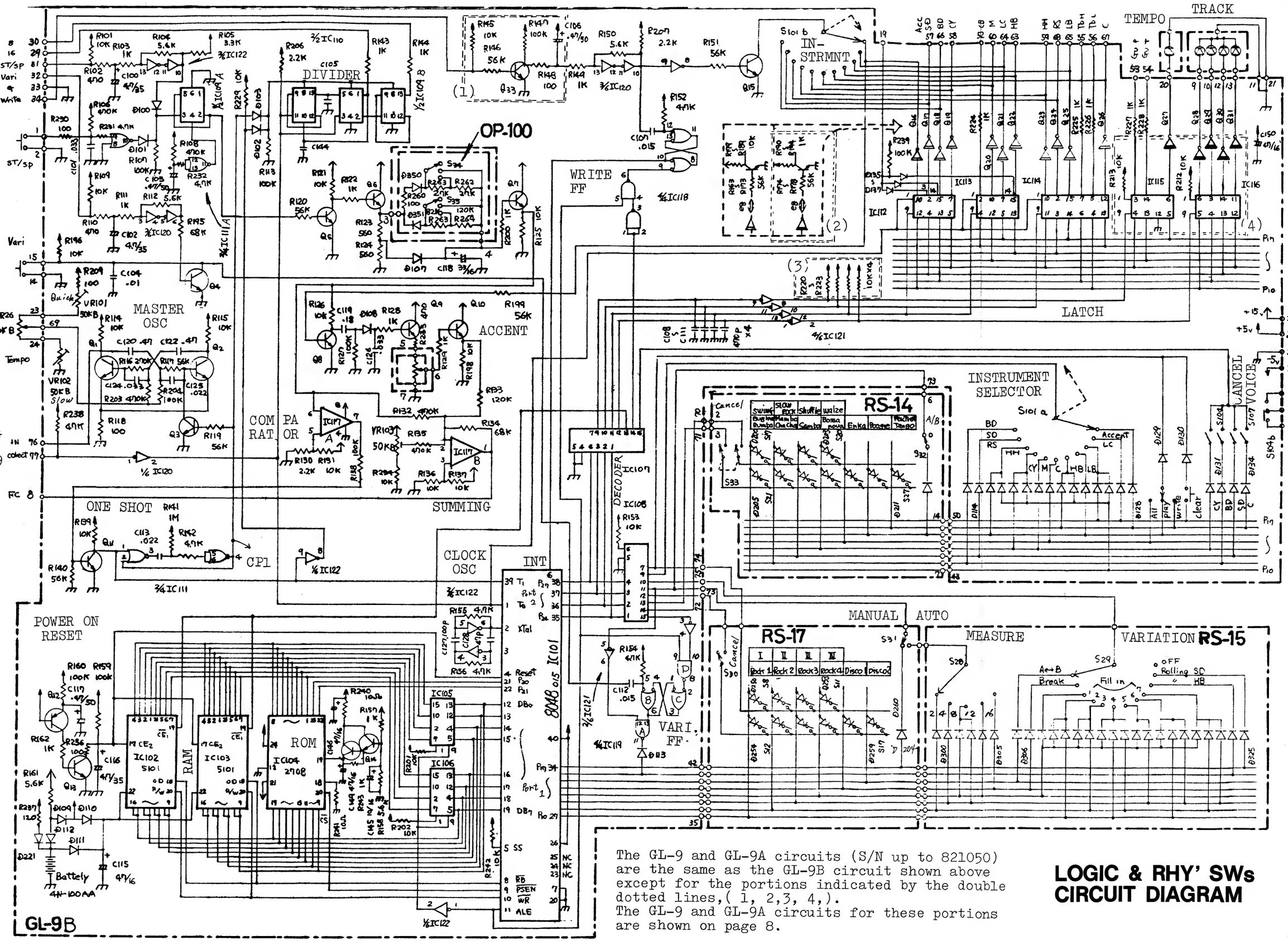
RS-17 (148-017)
(Etch mask 052-446)
view from foil side



GL-9B (142-009B)
(Etch mask 052-438B)
Serial No. 821051 and higher

IC101	μPD8048-015	IC109-110	MC14013B	IC60-122	74LS04
IC102-103	μPD5101C-E	IC111	MC14001B	IC112-113 IC115-116	74LS175 or MC14175B
IC104	Am2708DC-023	IC114	74LS174	Q12	2SA1015Y
IC105-106	74LS175	IC117	μPC4558C	Q (except Q12)	2SC1815GR
IC107-108	74LS138	IC118-119	74LS00	D	1S1588
				LD	SLP131B





The GL-9 and GL-9A circuits (S/N up to 821050) are the same as the GL-9B circuit shown above except for the portions indicated by the double dotted lines,(1, 2,3, 4,).
The GL-9 and GL-9A circuits for these portions are shown on page 8.

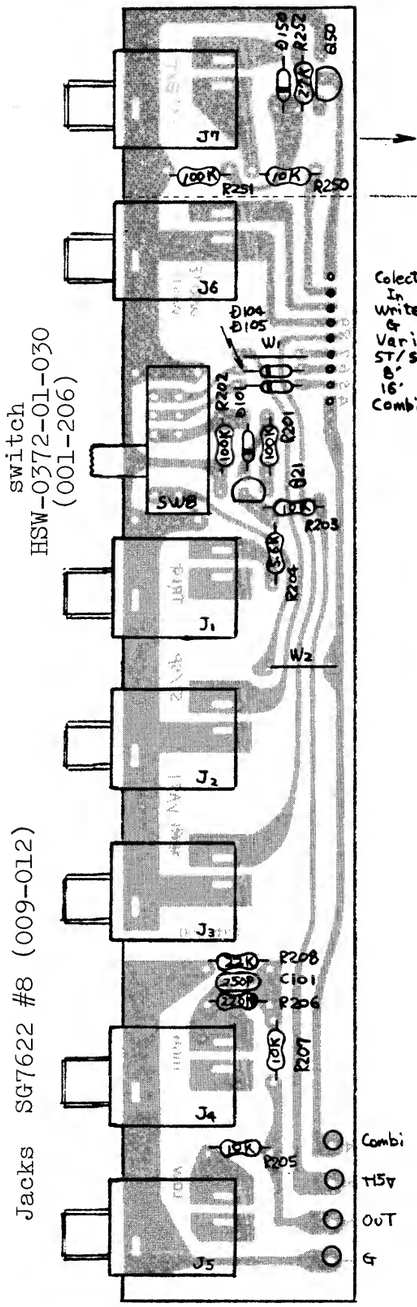
LOGIC & RHY' SWs CIRCUIT DIAGRAM

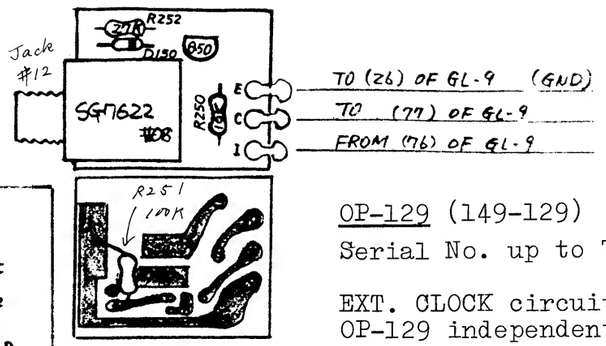
VG-11A (143-011A) (Etch mask 052-437A) Serial No. 780700 and higher

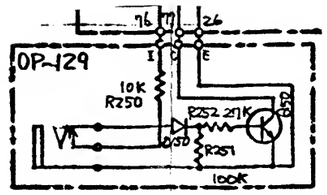
Q501-513	2SC900-F	IC501	MC14069
Q514-532	2SC1815-GR	IC502	BA662
Q533	2SC828-R(NZ)	IC503	μA78M05
Q534-535	2SA1015-Y	IC504	μA78M15
D500-526	1S1588	IC505	μA78L05

Components on foil side:

VG-11 - R645, C592
VG-11A- D533

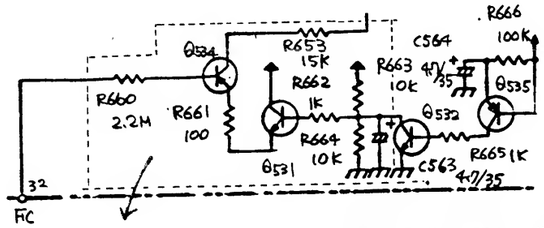


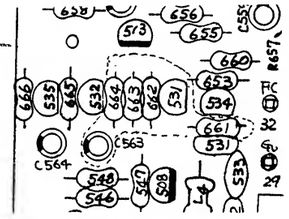




OP-129 (149-129)
Serial No. up to 780699

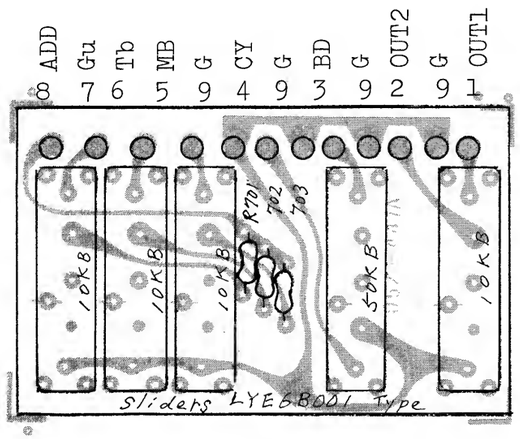
EXT. CLOCK circuit is arranged on OP-129 independently of OP-104.



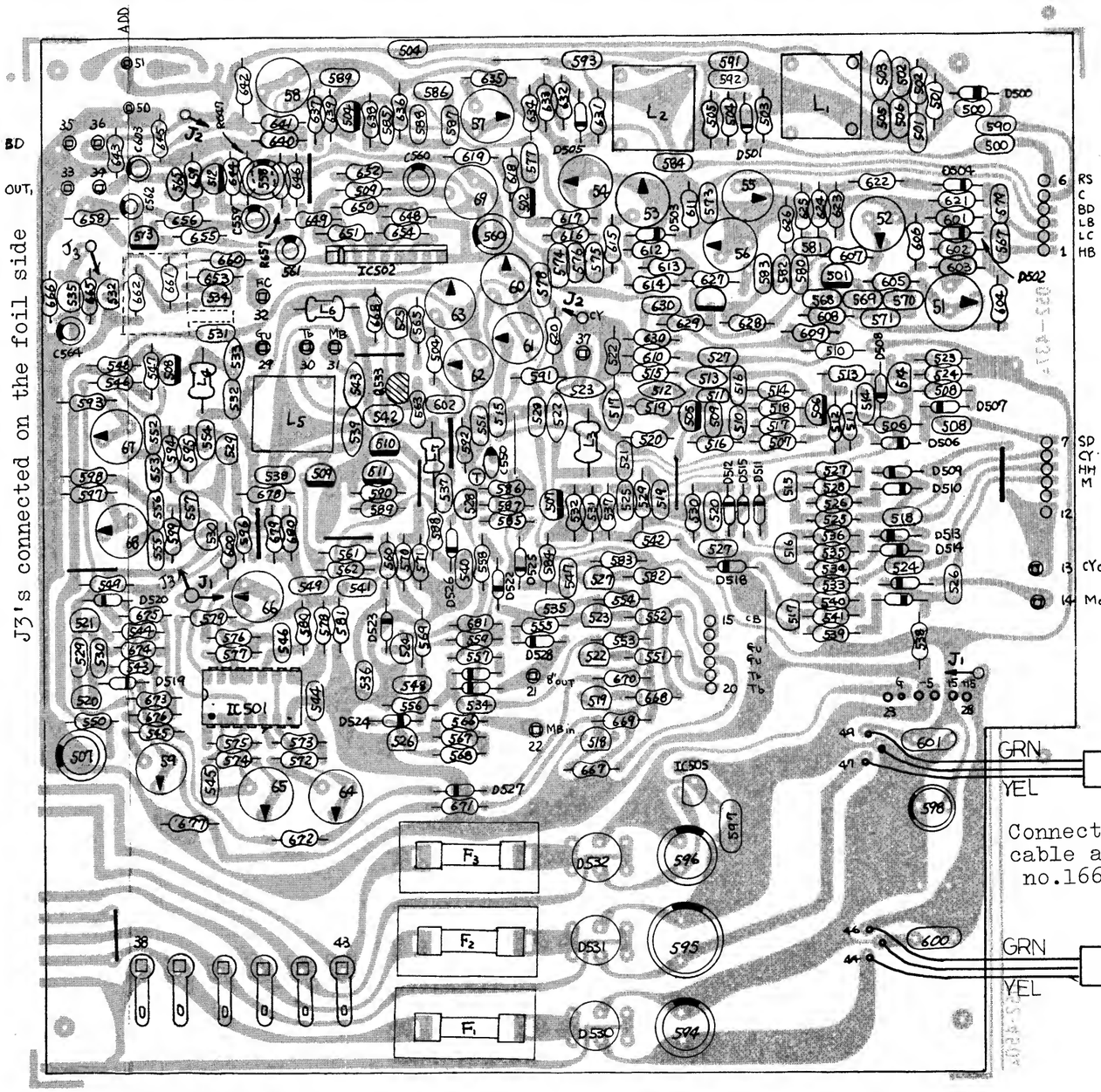


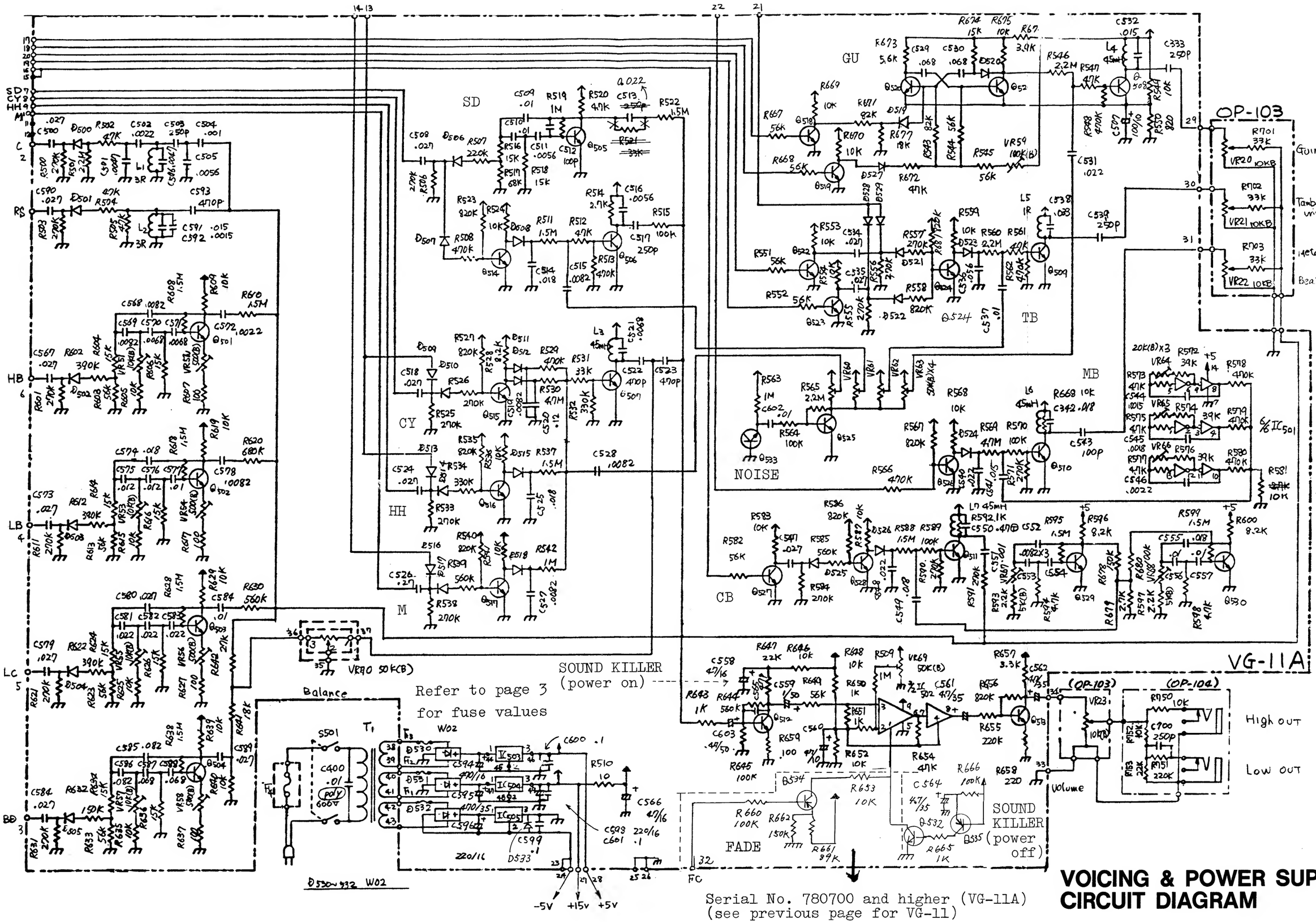
In the dotted lines shown are circuit configuration and components of VG-11 (S/N up to 780699), remainnings are almost the same as those on VG-11A which can replace the VG-11.

OP-103A (149-103A) (Etch mask 052-447A) view from foil side



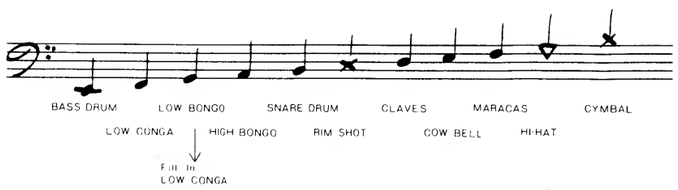
OP-104A (149-104A) (Etch mask 052-464) Serial No. 780700 and higher



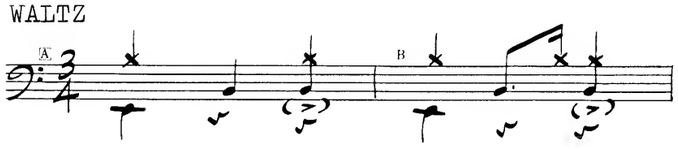


VOICING & POWER SUPPLY CIRCUIT DIAGRAM

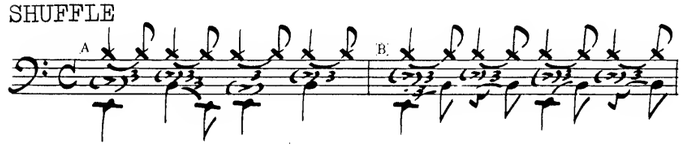
RHYTHM PATTERNS



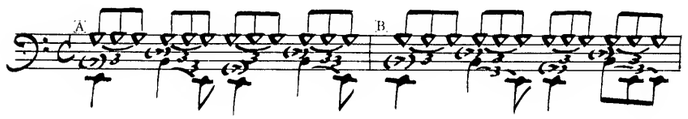
WALTZ



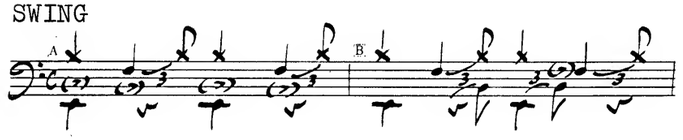
SHUFFLE



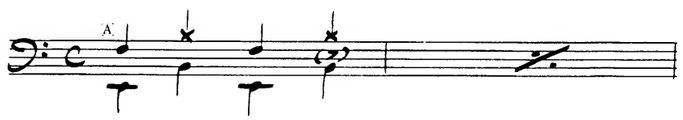
SLOW ROCK



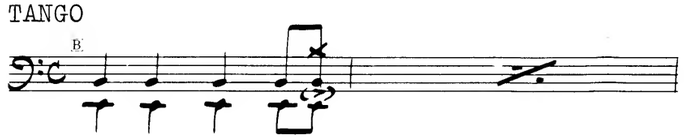
SWING



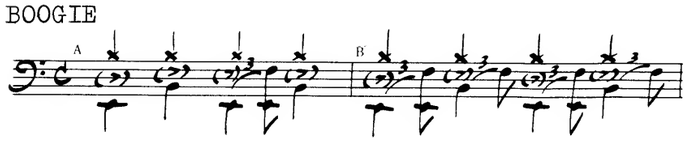
FOX TROT



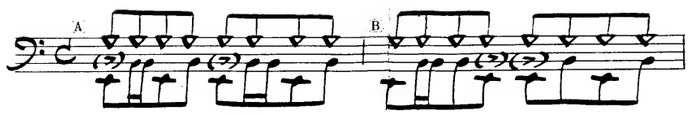
TANGO



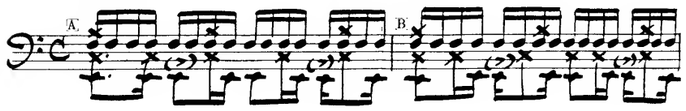
BOOGIE



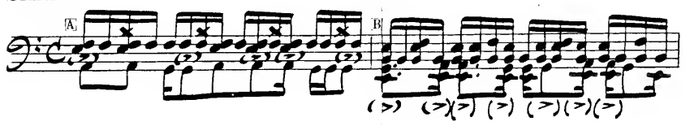
ENKA



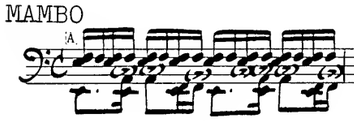
BOSSA NOVA



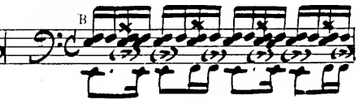
SAMBA



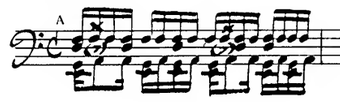
MAMBO



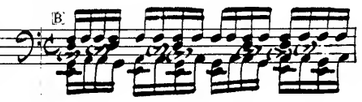
CHA CHA



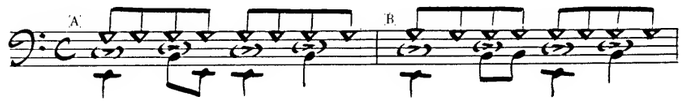
BEGUINE



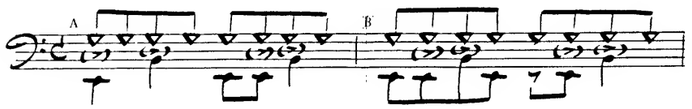
RHUMBA



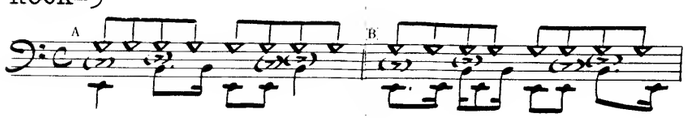
ROCK-1



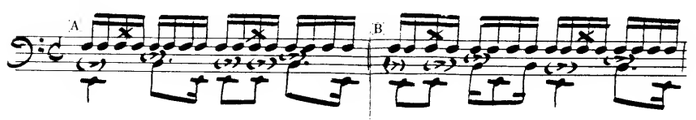
ROCK-2



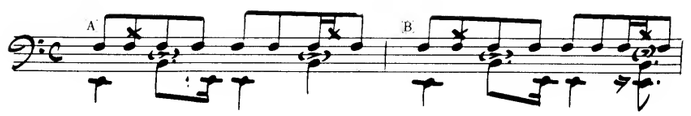
ROCK-3



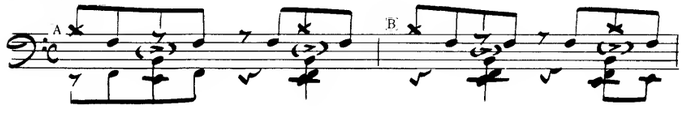
ROCK-4



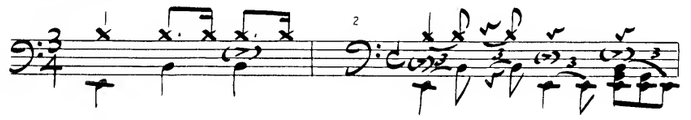
DISCO-1

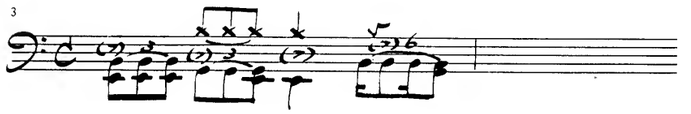


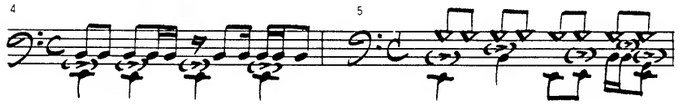
DISCO-2

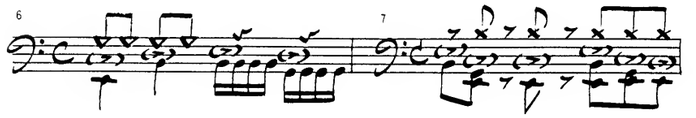


FILL IN









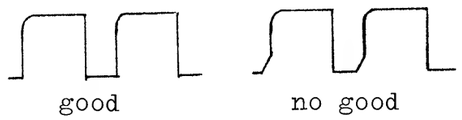
ADJUSTMENT & CHECKING

1. MASTER OSCILLATOR FREQUENCY (RHYTHM TEMPO)

Connect an oscilloscope to Q1 collector or pin 76 on GL-9.

1-1. Set TEMPO knob to full clockwise position (10).
Adjust VR101 for T = 10ms.

1-2. Turn the TEMPO control fully counterclockwise.
Adjust VR102 for T = 10ms.
Bottom half must be perfectly square.



2. FADE TIME

To be adjusted after step 1 is finished.
With rhythm (may be SAMBA-B) running, turn TEMPO fully clockwise.
Set FADE OUT to SHORT.
Depress START/STOP button.

2-1. When sound becomes inaudible, count the number of LED flashes until the LED stays on steadily.
Factory set ranges 4 (1.5sec) to 55 (2.4sec).

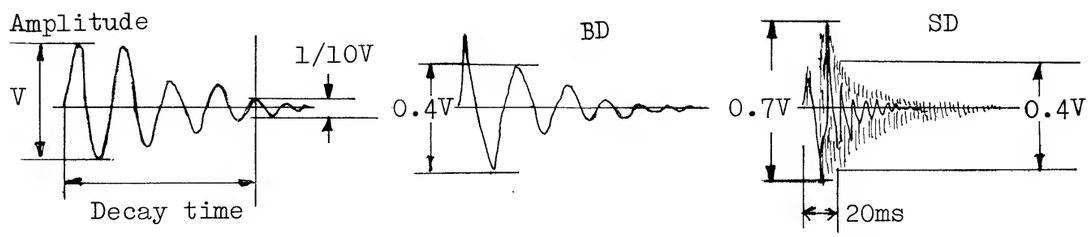
2-2. To adjust, turn VR103 on GL-9.

3. RHYTHM VOICE

Figures in the table at the right show factory standard and may be slightly deviated for personal taste or to meet frequency response of an amplifier being used.

Set all rhythm buttons to "off".
Depress START/STOP button to start the rhythm.

VOICE to be adjusted	Oscilloscope H IN	Oscilloscope V IN	Frequency Adjust	Frequency for ms	Frequency for Hz	Remark (-) non-adjustable: just check	Decay time Adjust	Decay time for ms	Amplitude Adjust	Amplitude for Vpp
To gate each VOICE circuit, BD through LC: connect TS-1 to WRITE jack and tap it as necessary with INSTRUMENT SELECTOR set to the voice to be adjusted.										
BD	connect to Q15 collector with TRIG. set at EXT.	connect to pin 34 on VG-11	VR57	16	62.5	w BALANCE set to the lowest	VR58	100	—	0.4
SD			—	3.0	340(Drum)		—	60	VR61	0.4
RS			—	6.67	1480		—	5	—	0.8
HH			Move BALANCE knob to the highest.			Adjusting VR60 on any one VOICE makes all.	—	60	VR60	0.4
CY							—	350		0.4
M							—	20		0.4
C				0.43	2630		—	18	—	0.15
HB			VR51	1.66	600		VR52	40	—	0.15
LB			VR53	2.5	400		VR54	40	—	0.15
LC			VR55	4.8	208		VR56	150	—	0.3
To gate CB voice circuits, short Q527 (on VG-11) across C-E momentarily.										
CB H	reset TRIG. to INTERNAL	Q529 collector	VR67	1.25	800	Shift scope V IN to pin 34 on VG-11	—	60	—	0.2
CB L		Q530 collector	VR68	1.8	555					
Slide ADD VOICE knobs upward,(Tb, GU, MB, respectively). Push in CYMBAL-HIGH HAT (CANCEL VOICE) when adjusting MB.										
Tb		Pin 34 on VG-11	—	—	—		—	220	VR62	0.25
GU H			VR59	8.0	125		—	—	VR63	0.3
GU L			VR59	13.0	77					
MB H		IC501 pin 8	VR64	0.162	6170	Shift scope V IN to pin 34 on VG-11	—	50	—	0.35
MB M		IC501 pin 4	VR65	0.178	5620					
MB L		IC501 pin 10	VR66	0.245	4080					



PARTS LIST

081-113	Cabinet no.117
111-020	Base no.20 (foot)
072-235	Panel no.235
076-356	Name plate no.356 rear OUTPUT-COMBI.
076-367	Name plate no.367 rear EXT. CLOCK-WRITE
061-218	Chassis no.218 front
061-219	Chassis no.219 main
061-220	Chassis no.220 rear
061-234	Chassis no.234 sub
061-235	Chassis no.235 sub
061-236	Chassis no.236 sub

KNOBS. BUTTONS

016-043	Knob no.43 TEMPO
016-044	no.44 FILL. MEASURE. INSTRUMENT. ACCENT
016-080	No.80 CLEAR. CANCEL
016-081	No.81 power switch
016-048	No.48 slider
016-067	No.67 MEMORY-ALL
016-008	Button No.8 gray
016-085	No.85 white
016-086	No.86 red
016-087	No.87 green
016-088	No.88 yellow
016-089	No.89 blue

COILS. TRANSFORMERS

022-030	Coil no.30 45mH
022-031	no.31 1R
022-033	no.33 3R 700mH
022-124N	PT no.124N 100V
022-124C	PT no.124C 117V
022-124D	PT no.124D 220/240V

TRANSISTORS

017-105	2SA1015-Y
017-106	2SC1815-GR
017-021	2SC900-F
017-046	2SC828-R (NZ) for noise

ICs

179-022	μPD8048C-015 computer

There are some versions of 8048. Each has an exclusive resident program.
Specify 8048C-015 for the CR-78 replacement.

179-023	AM2708P-023 ROM
020-181	μPD5101C-E RAM
020-141	*74LS175N (TTL)
020-196	*14175B or 74C175 (MOS) *refer to GL-9A parts layout
020-064	μPC4558
020-180	74LS174N
020-138	74LS138N
020-124	74LS04N
020-120	74LS00N
020-084	MC14069BCP
020-041	MC14013BCP
020-169	MC14001BCP
020-160	BA-662B VCA
020-073	μA78M15 regulator +15V
020-197	μA78M05 or μA7805 +5V
020-198	μA78L05 -5V

DIODES

018-059	1S1588
018-082	W-02 bridge 1.5A
019-013	SLP-131B LED red

SWITCHES

001-215	Power SDG-5P 100V
001-216	SDG-5P 117V
001-217	SDG-5P 220/240V
001-273	KCA10037 keyboard
001-206	HSW-0372-01-030 slide 8,16,COMBI
001-243	SRM1025 rotary MEASURE
001-242	SRM101C rotary FILL IN
001-239	SUFA2 push gang ROCK-DISCO 2
001-240	SUFB2 push gang WALTZ-
001-231	SLR322 lever Rhythm A/B. AUTO/MANU.
001-245	SLR323 lever FADE IN/OUT
001-246	SLR823 lever MEMO/PLAY/ALL
001-241	SUF53 1push gang CLEAR. CANCEL VOICE
001-244	SRA202B rotary INSTRUMENT

PCBs

143-011A	VG-11A(etch mask 052-437A)
142-009B	GL-9B (052-438B)
148-014	RS-14 (WALTZ-)(052-445)
148-015A	RS-15A (VARI.MEASURE) (052-444A)
148-017	RS-17 (PROGRAM. ROCK-) (052-446)
149-100A	OP-100A (052-449A)
149-103A	OP-103A (052-447A)
149-104A	OP-104A (052-464) (use 104A as a replacement for OP-129)

For the replacement, use PCBs listed above, interchangeable improved versions.

POTENTIOMETERS

026-024	EVHC0AP25B15 100KB TEMPO
026-021	EVHC0AP24B14 10KB ACCENT
029-410	LYE6B001-10KB VOL. ADD VOICE
029-411	LYE6B001-50KB BALANCE

Trimmers

028-001	EVTR4A00 (SR19) 500
028-003	EVTR4A00 (SR19) 5K
028-004	EVTR4A00 (SR19) 10K
028-005	EVTR4A00 (SR19) 20K
028-006	EVTR4A00 (SR19) 50K
028-007	EVTR4A00 (SR19)100K

CAPACITORS

032-095	0.47mfd 35V K tant.
035-109	ECQM6103KZ 600V polyester

FUSES. FUSE CLIP

008-024	SGA 0.5A prim. sec +5V 100/117V
008-026	SGA 1A sec +15V 100/117V
008-022	SGA 0.125A sec -5V 100.117V
008-053	CEE T50mA sec -5V 220/240V
008-060	CEE T250mA sec +15V 220/240V
008-062	CEE T400mA sec +5V 220/240V
008-060	CEE T250mA prim/sec +15V 220/240V
012-003	Clip TF-758

MISCELLANEOUS

009-012	Jack SG7622

IC Sockets

012-040	ICC30-040-350G	40-pin
012-041	ICC30-024-350G	24-pin
012-042	ICC30-022-350G	22-pin
047-003	Line cord strain relief BU4801	
047-023	Cord clamp 1702B	
120-001	Long nut (spacer/stand off) no.1 3x10mm	

PARTS ORDERING INFORMATION

When ordering parts, be sure to include the following information:

1. Model and Serial Number
2. Part Number
3. Part Name

If the necessity for a non-listed part arises, please write describing the parts location and function as well as model and serial number of the unit.

CR-78 MANUAL CHANGE INFORMATION

RECHARGEABLE BATTERY CHANGE

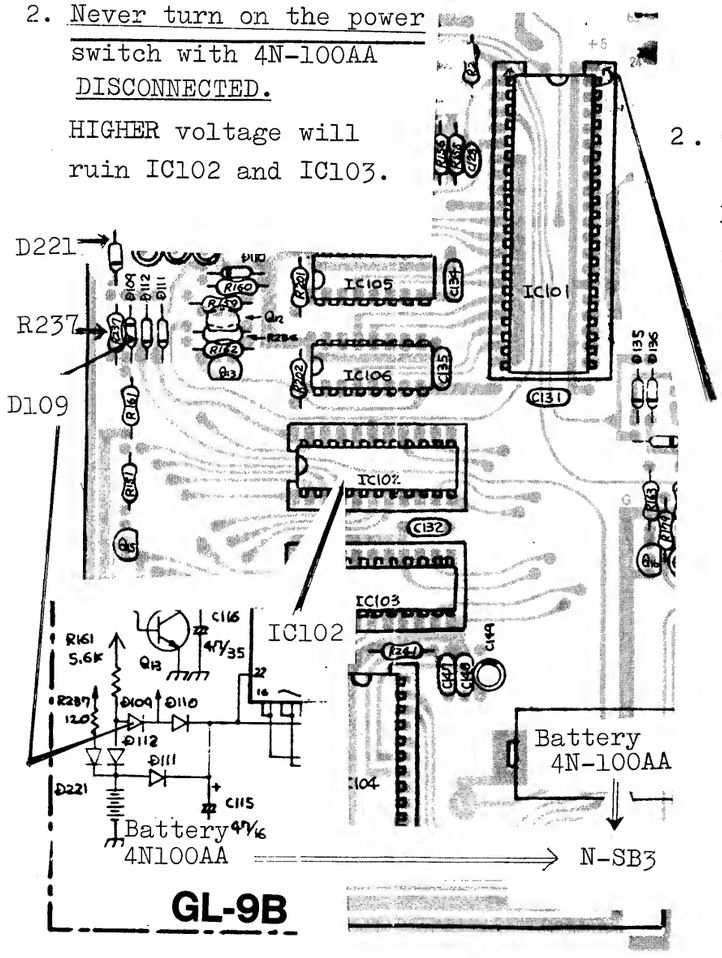
4N-100AA (5.6V)	to	N-SB3 (3.6V)
Serial no. up to 862899		Serial no. 872900 and higher
(no name is given on the face of the battery)		(name is definitely printed on the face)

GL-9 with 4N-100AA

1. D109 is removed at the factory to increase charging current. However, there are some products having D109 on the market. REMOVE D109 on the first ocassion.

(after D109 removed)

2. Never turn on the power switch with 4N-100AA DISCONNECTED. HIGHER voltage will ruin IC102 and IC103.

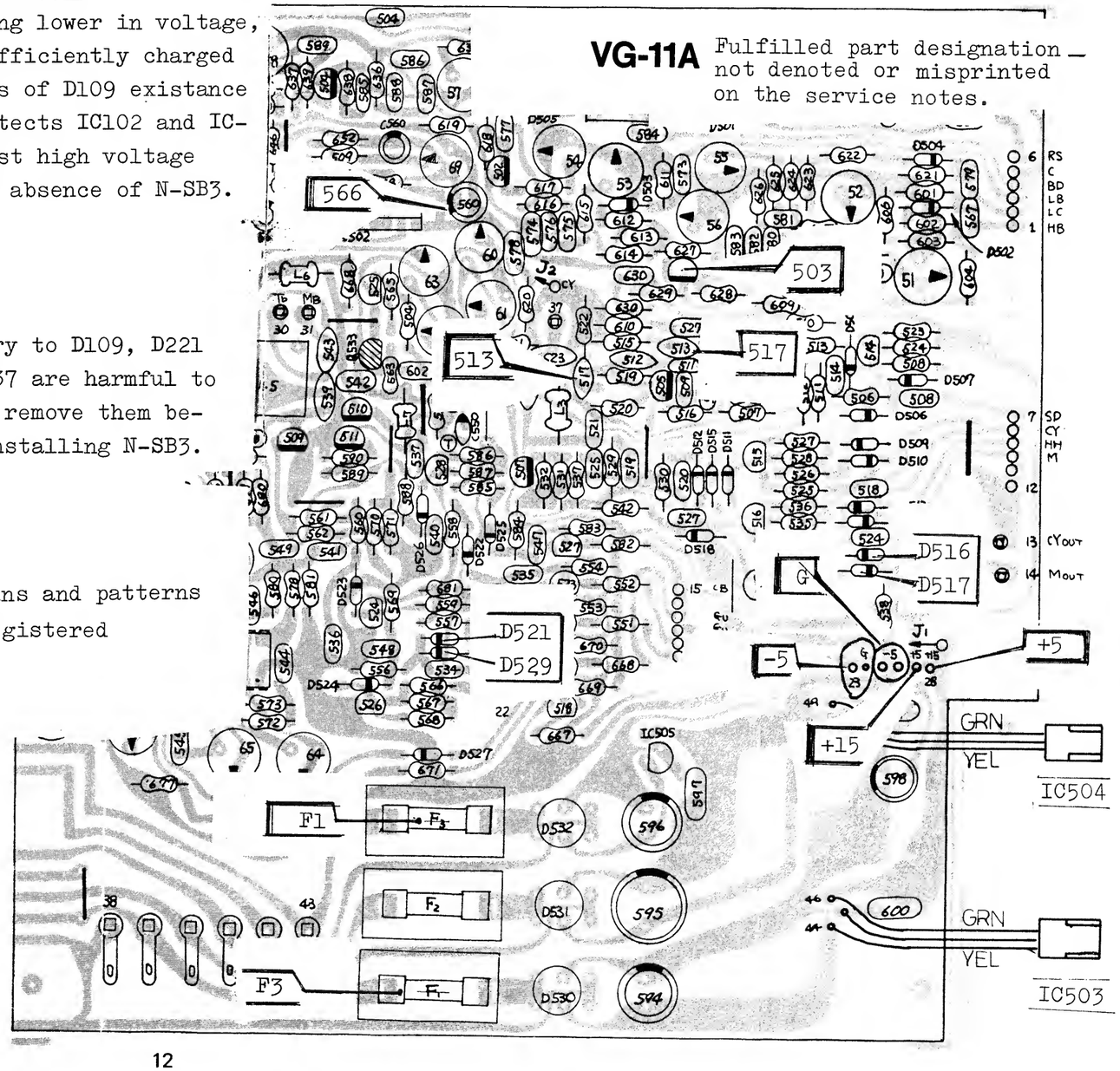


GL-9 with N-SB3

1. N-SB3 being lower in voltage, can be sufficiently charged regardless of D109 existance which protects IC102 and IC-103 against high voltage during an absence of N-SB3.

2. Contrary to D109, D221 and R237 are harmful to N-SB3, remove them before installing N-SB3.

IC pins and patterns misregistered



CORRECTION

ADJUSTMENT page 15

1-2. T = 10ms ------ 200ms
2-1. 4 to 55 ------ 4 to 5